APPENDIX

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An electrical signal regenerator comprising:

an equalizer;

a clock data recovery circuit; ~~and~~

a switch; and

a decision circuit for deciding upon a logical signal value 0 or 1,

wherein the decision circuit is connected to an output of the switch, and

wherein said switch is operable to either connect the clock data recovery circuit to an output of the electrical signal generator when an input signal of a higher bitrate multiplex signal is detected by the clock data recovery circuit, or bypass the data recovery circuit and connect the equalizer to the output of the electrical signal generator when an input signal of a lower bitrate multiplex signal is detected by the clock data recovery circuit.

2. (original): An electrical signal regenerator according to claim 1, wherein the clock data recovery circuit comprises a detector for detecting the bitrate of the input signal.

3. (canceled)

4. (original): An electrical signal regenerator according to claim 1, comprising a test loop controllably connectable from the output to the input of the regenerator.

5. (original): An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a tapped delay line.

6. (previously presented): An electrical signal regenerator according to claim 1, wherein said equalizer being an analogue equalizer comprising a first tap and a second tap, the first tap having a higher delay than the second tap, both taps being connected to a adder-subtractor for generating a signal corresponding to a difference between output signals of the first and second taps.

7. (previously presented): : An electrical signal regenerator according to claim 6, wherein the signal ratio between the two taps is adjustable.

8. (previously presented): An electrical signal regenerator according to claim 6, wherein the signal ratio between the two taps is adjustable, and wherein the ratio is determined by two peak detectors.

9. (currently amended): A network element, comprising internal electrical signal paths, wherein at least part of said paths are terminated by an electrical signal regenerator comprising:

an equalizer; ~~and~~

a clock data recovery circuit; ~~and~~

a switch; and

a decision circuit for deciding upon a logical signal value 0 or 1,

wherein the decision circuit is connected to an output of the switch, and

wherein said switch is operable to either connect the data recovery circuit to an output of the electrical signal generator when an input signal of a higher bitrate multiplex signal is detected by the clock data recovery circuit, or to bypass the data recovery circuit and connect the equalizer to the output of the electrical signal generator when an input signal of a lower bitrate multiplex signal is detected by the clock data recovery circuit.

10. (original): A network element according to claim 9 being an optical crossconnect comprising an electrical space switching matrix, said matrix comprising a number of switch

modules being interconnected by means of internal electrical cables, an electrical signal regenerator is coupled to one end of each internal electrical cable in front of a switching module.

11. (previously presented): A network element according to claim 10, wherein said switching modules being adapted to output a test signal at each unused output port and wherein the electrical signal regenerator is adapted to raise an alarm when neither a test signal nor a valid input signal is detected.

12. (currently amended): A method of transmitting an electrical signal having either a first or a second bitrate, wherein the first bitrate is higher than the second bitrate, said method comprising the steps of

transmitting said electrical signal via a signal path;

detecting the bitrate of said electrical signal received from the signal path;

in the case the electrical signal has the first bitrate, performing a first regeneration of said electrical signal and then performing a second regeneration; ~~and~~

in the case the signal has the second bitrate, performing said first regeneration of said signal, only, wherein the detecting the bitrate of said electrical signal is performed by a unit performing the second regeneration; and

deciding upon a logical signal value 0 or 1 with respect to an output of said first regeneration and second regeneration, and an output of said first regeneration of said signal only.

13. (original): A method according to claim 12, wherein said first signal regeneration is an electrical equalization and wherein said second signal regeneration is a clock data recovery.

14. (previously presented): An electrical signal regenerator according to claim 4, wherein a static test signal is fed via the test loop to an input of the equalizer while no external signal is input to the input of the equalizer.

15. (previously presented): An electrical signal regenerator according to claim 8, wherein a first detector of the two peak detectors is connected to an input of the equalizer to detect a static test input signal, and a second detector of the two peak detector is connected to an output of the first tap.

16. (previously presented): An electrical signal regenerator according to claim 1, wherein the higher bit rate is approximately 10 Gbit/s and the lower bit rate is approximately 2.7 Gbits/s.